Dynamic Logic

Adapted from:
CMOS Logic Circuit Design by John P. Uyemura, 2002

Dynamic CMOS

- In **static** circuits at every point in time (except when switching) the output is connected to either GND or $V_{DD}$ via a low resistance path.
  - fan-in of $n$ requires $2n$ ($n$ N-type + $n$ P-type) devices

- **Dynamic** circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.
  - requires on $n + 2$ ($n+1$ N-type + 1 P-type) transistors
Dynamic (Precharge/Evaluate) Logic Gate

Precharge Phase
Evaluate Phase

(a) $C_{out}$ discharges

(b) Charge held on $C_{out}$

Conditions on Output

- Once the output of a dynamic gate is discharged, it cannot be charged again until the next precharge operation.
- Inputs to the gate can make at most one transition during evaluation.
- Output can be in the high impedance state during and after evaluation (PDN off), state is stored on $C_l$.
Properties of Dynamic Gates

- Logic function is implemented by the PDN only
  - number of transistors is \( N + 2 \) (versus \( 2N \) for static complementary CMOS)
- Full swing outputs \( (V_{OL} = \text{GND} \text{ and } V_{OH} = V_{DD}) \)
- Non-ratioed - sizing of the devices does not affect the logic levels
- Faster switching speeds
  - reduced load capacitance due to lower input capacitance \( (C_i) \)
  - reduced load capacitance due to smaller output loading \( (C_{out}) \)

Properties of Dynamic Gates

- Overall power dissipation usually higher than static CMOS
  - no static current path ever exists between \( V_{DD} \) and GND
  - no glitching
  - higher transition probabilities
  - extra load on Clk
- PDN starts to work as soon as the input signals exceed \( V_{Th} \), so \( V_M, V_{IH} \) and \( V_L \) equal to \( V_{Th} \)
  - low noise margin \( (NM_L) \)
- Needs a precharge/evaluate clock
### Issues in Dynamic Gates: Charge Sharing

![Diagrams showing charge sharing and precharge network](image)

Cout must share charge with C1 and C2.  
\[ V_f = V_{DD} \left( \frac{C_{out}}{C_{out} + C_1 + C_2} \right) \]

### Issues in Dynamic Gates: Charge Leakage

![Diagram showing charge leakage](image)

After charge redistribution takes place, the value of Vout continues to fall because of charge leakage.
Summary

The most important feature of this type of dynamic logic gate is that the clock controls the precharge and evaluate sequence, and hence synchronizes the data flow through a cascade that consists of similar gates. The problems of discharge time constants, charge sharing, and charge leakage are the most critical aspects of the circuit behaviour.

Examples of Dynamic Gates

![Diagram of dynamic gates](attachment:image.png)
Examples of Dynamic Gates

Functions?

Cascading Dynamic Gates
Problem with Cascading Dynamic Gates

Correct operation is guaranteed as long as the inputs can only make a single 0 -> 1 transition during the evaluation period. Setting all inputs of the second gate to 0 during precharge will fix the problem.

Cascading Dynamic Gates

Only $0 \rightarrow 1$ transitions allowed at inputs!
**Domino Logic**

Evaluate transitions

**Why Domino?**

Like falling dominos!
Properties of Domino Logic

- Only non-inverting logic can be implemented
- Very high speed
  - static inverter can be skewed, only L-H transition
  - Input capacitance reduced – smaller logical effort

Differential (Dual Rail) Domino

Solves the problem of non-inverting logic
np-CMOS

Only 0 → 1 transitions allowed at inputs of PDN
Only 1 → 0 transitions allowed at inputs of PUN